What is claimed is:

1. A semiconductor memory device comprising:

a test means for performing a test operation for an alternative one of row and column, detecting defective cells on the alternative unit of the row and column; and

a repair analysis means for performing a repair analysis in which a fail address data involved in defective cells on the alternative one of the row and column are rearranged with including moving and exchanging between the fail address data in a unit of row and column.

2. The device of claim 1, wherein the repair analysis means includes:

a temporary buffer unit having a plurality of temporary buffers for storing the fail address data for the defective cells;

a data buffer receiving the fail address data stored in one of the temporary buffers;

a storage means receiving the fail address data from the data buffer and for rearranging a structure of the fail address data; and

a controller for controlling operations of the temporary buffer unit, the data buffer and the data storage means.

3. The device of claim 2, wherein the temporary buffer unit includes:

the temporary buffers for storing the fail address data detected by the test means;

an input selector for transferring the fail address data into an alternative one of the temporary buffers from the test means;

an output selector for transferring the fail address data to the data buffer from an alternative one of the temporary buffers; and

a controller for controlling operations of the input and output selectors.

4. The device of claim 3, wherein the temporary buffer includes:

a main register for storing main address data determined by a scanning type of the test operation;

a plurality of sub registers for storing sub address data determined by a scanning type of the test operation; and

a flag registers for storing a flag informing of a presence of data in the main register.

5. The device of claim 2, wherein the data buffer includes:

a main register for storing main address data determined by a scanning type of the test operation; and

a plurality of sub registers storing sub address data determined by a scanning type of the test operation.

6. The device of claim 2, wherein the data storage means includes:

an entry storage block for storing the fail address data; and

a function block for operating the rearrangement operation for the fail address data stored in the entry storage block.

7. The device of claim 6, wherein the entry storage block includes a plurality of entry registers for storing the fail address data.

8. The device of claim 7, wherein each of the entry registers includes:

a main entry store for storing a main entry address data;

a main state flag store for storing a flag informing of status of the main entry store;

a plurality of sub entry stores for storing sub entry address data;

a plurality of sub state flag store for storing flags informing of status of the sub entry stores; and

a fix flag store for storing a fix flag for settling an alternative one of a redundant row and a redundant column designated by the main entry address data.

9. The device of claim 6, wherein the function block includes:

a plurality of data comparators for comparing between the data stored in the data buffer and the data stored in the entry storage block; and

a data state comparator for combining output signals supplied from the data comparators and applying the combined signals to the controller.

10. A semiconductor memory device having a repair analysis means for fail address data

assigned to defective cells on an alternative one of row and column and detected by performing a scanning test for the alternative one of the row and column, includes;

a temporary buffer unit having a plurality of temporary buffers storing the fail address data for the defective cells;

a data buffer receiving the fail address data stored in one of the temporary buffers;

a data storage means receiving the fail address data from the data buffer and rearranging a structure of the fail address data; and

a controller for controlling operations of the temporary buffer unit, the data buffer and the data storage means.

11. The device of claim 10, wherein the temporary buffer unit includes:

the temporary buffers for storing the fail address data;

an input selector for transferring the address data to an alternative one of the temporary buffers;

an output selector for transferring the fail address data to the data buffer from an alternative one of the temporary buffers; and

a controller for controlling selection operations of the input and output selectors.

12. The device of claim 11, wherein the temporary buffer includes:

a main register for storing a main address data determined by a scanning type of the test operation;

a plurality of sub registers for storing a sub address data determined by a scanning type of the test operation; and

a flag register for storing a flag informing of a presence of data in the main register.

13. The device of claim 10, wherein the data buffer includes:

a main register for storing the main address data determined by a scanning type of the test operation; and

a plurality of sub registers for storing the sub address data determined by a scanning type of the test operation.

14. The device of claim 10, wherein the data storage means includes:

an entry storage block for storing the fail address data; and

a function block for performing the rearrangement for the structure of the fail address data.

15. The device of claim 14, wherein the entry storage block includes a plurality of entry registers for storing the fail address data.

16. The device of claim 15, wherein each of the entry registers includes:

a main entry store for storing a main entry address data;

a main state flag store for storing a flag informing of status of the main entry store;

a plurality of sub entry stores for storing sub entry address data;

a plurality of sub state flag stores for storing flags informing of status of the sub entry stores; and

a fix flag store for storing a fix flag for settling an alternative one of a redundant row and a redundant column designated by the main entry address data.

17. The device of claim 14, wherein the function block includes:

a plurality of data comparators for comparing the data stored in the data buffer and the data stored in the entry storage block; and

a data state comparator for combining output signals supplied from the data comparator and applying the combined signal to the controller.

18. A method of performing a repair analysis with fail address data assigned to defective cells on an alternative one of row and column in a semiconductor memory device, comprising:

storing the fail address data for defective cells detected in the test step for the alternative one of the row and column into a temporary buffer unit;

storing the fail address data stored in the temporary buffer unit into a data buffer;

writing the fail address data stored in the data buffer into the storage block; and

moving and exchanging the fail address data stored in the storage block.

19. The method of claim 18, wherein the storing includes:

first transferring the coincident row fail address data and column fail address data associated with the coincident row fail address data into the data buffer, when the row fail address data stored in the storage block is coincident with the row fail address data stored in the temporary buffer unit,;

second transferring the coincident column fail address data and row fail address data associated with the coincident column fail address data into the data buffer, when the column fail address data stored in the storage block is coincident with the column fail address data stored in the temporary buffer unit,; and

third transferring the data of the temporary buffer unit into the data buffer, when the fail address data stored in the storage unit is different from the fail address data stored in the temporary buffer unit.

20. The method of claim 19, wherein the first transferring is operable in a condition of progressing a first test stage and a second test stage in sequence.

21. The method of claim 19, wherein the second transferring is operable in a condition of progressing an unique test stage.

22. The method of claim 19, wherein the second transferring is operable in a condition of progressing a first test stage and a second test stage in sequence.

23. The method of claim 18, wherein the repair analysis includes:

first transferring the data stored in the data buffer to first main entry stores of the storage block when the first main entry stores have emptied entry stores;

second transferring the data stored in the data buffer to the second main entry stores which have the coincident data, when the data stored in second main entry stores are coincident with the data stored in the first sub entry stores, wherein the first sub entry stores store column fail address data in the row scan test while row fail address data in the row scan test;

comparing the number of second sub entry stores associated with the first main entry stores of the storage block with the number of data stored in the first sub entry stores of the data buffer when it is unavailable to store the data of the data buffer into the storage block through the first and second storage steps;

writing the data stored in the first sub entry stores of the data buffer into the second main entry stores when the number of the second sub entry stores associated with the first main entry stores of the storage block is larger than that of the data stored in the first sub entry stores of the data buffer;

rearranging the data structure of the storage block when it is unavailable to store the data stored in the first sub entry stores of the data buffer into the second main entry stores of the storage; and

second rearranging the data structure of the storage block when the number of the second sub entry stores associated with the first main entry stores of the storage block is less than that of data stored in the first sub entry stores of the data buffer.

24. The method of claim 23, wherein the first transferring determines whether or not the first main entry stores and the second sub entry stores are being emptied, by using state flags.

25. The method of claim 23, wherein the second transferring is repeated when there are a plurality of data stored in the first sub entry stores of the data buffer.

26. The method of claim 23, wherein the number of the second sub entry stores corresponds to the number of valid state flags, in the comparison step.

27. The method of claim 18, wherein the rearranging includes:

first transferring data stored in the first main entry stores associated with the coincident data to first sub entry stores associated with the coincident data of the second main entry stores when the data stored in second sub entry stores associated with first main entry stores of the storage block are coincident with the data stored in second main entry stores; and

second transferring data stored in the first main entry stores associated with the

coincident data to first sub entry stores associated with the coincident data of the second main entry stores when the data stored in second sub entry stores associated with first main entry stores of the storage block are coincident with the data stored in second main entry stores.